

Appl. No. 09/876,290  
Amdt. Dated January 21, 2009  
Reply to Office Action of July 21, 2008

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**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A multilayer semiconductor device assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig, comprising:

~~a lateral position restriction structure for maintaining alignment of a plurality of stacked semiconductor modules with their respective lateral positions mutually restricted, the lateral position restriction structure~~ at least one pair of opposed side walls formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules located therebetween so as to rigidly restrict displacement of said semiconductor modules;

~~a removable height restriction mechanism disposed opposite said base member and which interfaces with said lateral position restriction structure for restricting an entire height of said semiconductor modules layered on said base member;~~

the jig having a mother substrate alignment pins located in the side walls structure for securing the mother substrate to the jig; and

further wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections ~~on~~ at a top and bottom surface thereof provided by solder located between conductive pads on adjacent printed wiring boards and wherein adjacent

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semiconductor modules are secured to one another by solder connections ~~between~~  
~~respective top and bottom surfaces thereof.~~

2. (Cancelled)

3. (Withdrawn) The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed in said rectangular-shaped member and said mother substrate.

4. (Withdrawn) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which are used for securing at least three different portions of an outer periphery of said semiconductor modules and at least two opposing sides of said semiconductor modules.

5. (Withdrawn) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which pierce through positioning holes formed in said semiconductor modules.

6. (Withdrawn) The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pins are aligned in a manner so as to also pierce through a  
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positioning hole formed in said mother substrate when the jig is mounted on the mother substrate.

7. (Cancelled)

Claims 8. - 10. (Canceled)

11. (Currently Amended) A multilayer semiconductor device assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig, comprising:

~~a lateral position restriction structure for maintaining alignment of a plurality of stacked semiconductor modules with their respective lateral positions mutually restricted, the lateral position restriction structure comprised of at least two opposed side walls having a single stack of the semiconductor modules therebetween, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules so as to rigidly restrict displacement of said semiconductor modules;~~

~~a removable height restriction mechanism disposed opposite said base member and which interfaces with said lateral position restriction structure for restricting an entire height of said semiconductor modules layered on said base member;~~

a mother substrate alignment structure comprised of pins located in the side walls secured to the jig;

and further wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board

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that has electrical connections ~~at on~~ a top and bottom surface thereof provided by solder located between conductive pads on adjacent printed wiring boards and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

12. (Withdrawn) The multilayer semiconductor device assembly jig of claim 11, wherein the alignment mechanism is comprised of a plurality of vertical pins secured in said base member.

13. (Withdrawn) The multilayer semiconductor device assembly jig of claim 11, wherein the alignment mechanism is further comprised of a plurality of vertical pins that pierce through the stacked semiconductor modules.

14. (Currently Amended) An assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig comprising:

~~two pairs~~ at least one pair of substantially parallel opposed side walls secured to a solid base member, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules ~~so as to rigidly restrict displacement of said semiconductor modules;~~

~~a removable cover member located opposite said base member and which interfaces with the side walls;~~

~~an internal void defined by said two pairs of opposed side walls providing a reception area for a plurality of semiconductor modules such that modules disposed within~~

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~~the void are aligned and their lateral motion is prevented by the side walls, and wherein the semiconductor modules are comprised of at least one chip and one wiring board;  
and further wherein the removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module~~

the plurality of semiconductor modules secured within the jig each being comprised of one or more semiconductor chips each secured to a printed wiring board that has electrical contacts at a top and bottom surface thereof and solder located between conductive pads on adjacent printed wiring boards and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

15. (Withdrawn) The assembly jig of claim 15, further comprising mother substrate alignment pins that extend through portions of the cover member and the side walls.

Claims 16. - 19. (Canceled)

20. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein said mother substrate alignment structure is formed ~~in said lateral position restriction mechanism~~ as a hole that receives a pin member.

Claim 21. (Canceled)